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ABSTRACT

This document presents information about the implementation of turbo codes. Turbo coding represents a new and very powerful error control technique, which has started to have a significant impact in the late 90s, allowing communication very close to the channel capacity. The powerful error correction capability of turbo codes was recognised and accepted for almost all types of channels leading to increased data rates and improved Quality of Service. Turbo codes can operate at 0.1 dB from the Shannon capacity limit outperforming any other coding technique known today.

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1. Introduction

This document presents information about the implementation of turbo codes. Turbo coding represents a new and very powerful error control technique, which has started to have a significant impact in the late 90s, allowing communication very close to the channel capacity. The powerful error correction capability of turbo codes was recognised and accepted for almost all types of channels leading to increased data rates and improved Quality of Service. Turbo codes can operate at 0.1 dB from the Shannon capacity limit outperforming any other coding technique known today [1].

The other equally important feature comes from the iterative decoding technique used for turbo decoding which can be extended to include the front end of the receiver, the synchronisation, equalisation and demodulation processes, all in a single loop with significant improvements in frequency selective channels or multiuser channels.

In the near future the digital turbo decoder will be replaced with its more refined relative, the analog decoder based on analog networks. Characterized by very low power consumption and high decoding speeds, this will represent an ideal solution for handheld terminals. From the source of information to its destination, analog communications all the way down!

Turbo codes were introduced in 1993 [2] and the first modem designed for a commercial application of turbo codes was tested in 1997 ([3], [4], [5], [6]).

A lot of research has been done in the application of turbo codes in deep space communications, mobile satellite/cellular communications, microwave links, paging, in OFDM and CDMA architectures. Turbo codes outperformed all previously known coding schemes regardless of the targeted channel. The extra coding gain offered by turbo codes can be used either to save bandwidth or reduce power requirements in the link budget.

Many standards based on turbo codes have already been defined or are currently under investigation. This paper attempts to summarise these applications and different turbo decoder implementations and refers the reader to more detailed references. It also discusses a few misconceptions related to the complexity, delay, sensitivity to signal-to-noise ratio (SNR), error floor and memory requirements of turbo codes.

The paper is organised in the following sections: Section 2 introduces the architecture of a turbo codec and the iterative decoding process; Section 3 describes some of the most common misconceptions regarding turbo codes; Section 4 describes application of turbo codes and their implementation; Section 5 presents a state-of-the-art solution for ADSL modems based on turbo codes. It includes an example explaining the advantages of using independent I & Q modulation and another example showing how the transmitter delay can be reduced, thus allowing larger interleaver sizes to be used.

2. Architecture

2.1 Block Diagram of the Turbo Codec

The turbo codec top-level architecture for a parallel concatenated scheme is shown Figure 1.

The incoming information bits, **d**, are encoded by a Rate 1/3 systematic turbo encoder. The outputs from the turbo encoder are the systematic bits **d**, the parity bits **p** and the parity bits **q**. The puncturing block determines the actual coding rate. The puncturing function is a simple deletion of some parity bits from the **p** and the **q** streams. No puncturing is applied to the information bits **d**.

The mapping function groups different information and parity bits together to produce the required amplitude for the I and the Q dimensions of the QAM signal. The I and the Q signals are then modulated and sent to the channel.

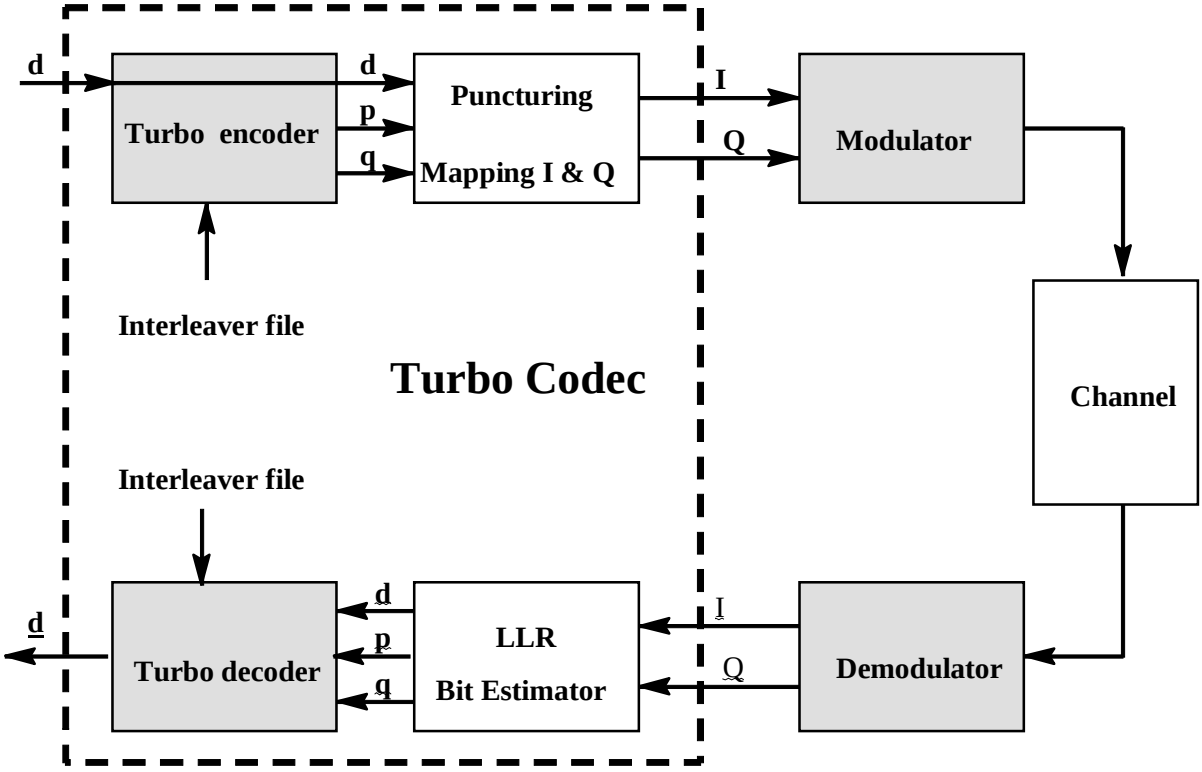

Figure 1: Communication System Block Diagram

At the receiver, after soft decision demodulation, the received I and Q signals are input to the bit estimator block. The function of this block is to compute the log-likelihood ratios (LLR) for each bit of the received QAM symbol. The outputs from this block are punctured streams of the estimated **d**, **p** and **q** bits. The turbo decoder doesn't need to know anything about what mapping or modulation scheme was transmitted. The same decoding engine is used to produce the decoded bits **d** regardless of the modulation or puncturing scheme used.

2.2 The Turbo Encoding/Decoding Process

Consider the generic rate 1/3 turbo encoder shown in Figure 2. The outputs of the turbo encoder are the information sequence $\mathbf{d_i}$, together with the corresponding parity sequence $\mathbf{p_i}$ produced by one encoder block, say **ENC1**, and the parity sequence $\mathbf{q_i}$ produced by the second encoder block, say **ENC2** . These sequences are modulated and sent through the channel. The interleaved data sequence, $\mathbf{Id_i}$, is not sent because it can be regenerated at the receiver by interleaving the received sequence corresponding to $\mathbf{d_i}$.

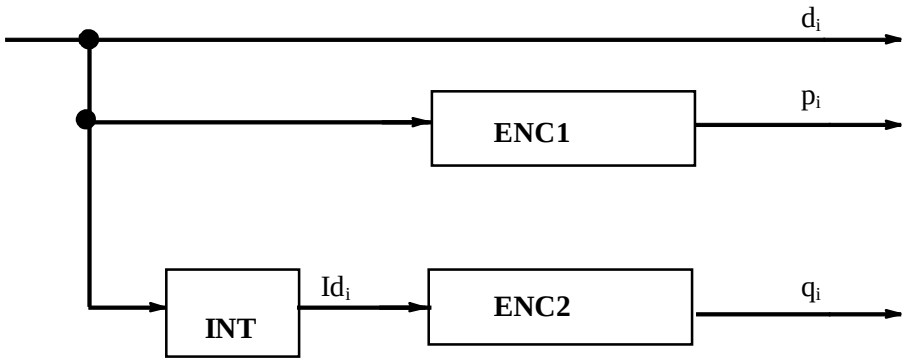

Figure 2: Generic rate 1/3 turbo encoder

At the receiver, turbo decoding is performed in an iterative process as it is shown in Figure 3.

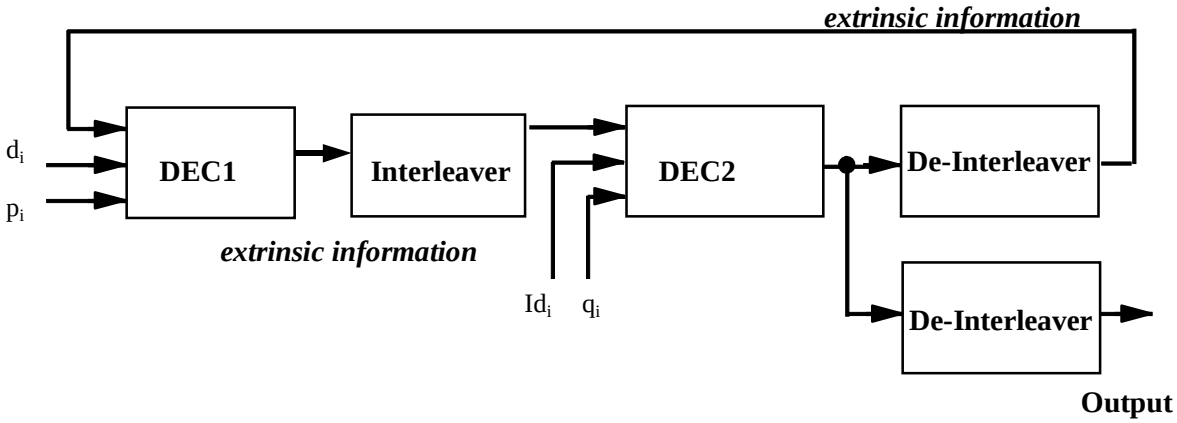

Figure 3: Generic turbo decoder

Decoder **DEC1** provides a soft output which is a measure of the reliability of each decoded bit. From this reliability information, the extrinsic information is produced, which does not depend on the current inputs to the decoder. This extrinsic information, after interleaving, is passed on to **DEC2** which uses this information to decode the interleaved bit sequence. From the soft outputs of **DEC2**, the new extrinsic information is fed back to the input of **DEC1** and so on.

3. Misconceptions

This section attempts to bring some light into some mistaken beliefs regarding the implementation of turbo codes in practical systems. Many studies done in the last few years have shown that properly designed turbo codes do not have any error floor, that they can perform at 0.1 dB from capacity, the decoder complexity is well within the capability of the current technology and the delay is not at all significant at data rates used currently in almost all communication systems.

3.1 SNR estimation

The first is the effect of SNR mismatch on the bit error rate (BER) performance. There are many papers discussing good variance estimators or modified decoding algorithms that can work without SNR estimators. From my practical experience ([3], [7]) and recent theoretical and simulation results [8], an accurate estimation of the SNR is not necessary. As a simple rule to remember, overestimating the SNR is better than underestimating and ± 2 dB inaccuracy in variance estimator do not translate in a measurable BER degradation. In [8] it was shown that if the channel is constant, it is good enough to use the SNR of the design point. If the actual SNR is smaller, the decoder will not be able to perform well anyway. If the actual SNR is higher, the BER will be better than anticipated. For a varying channel, a set of design points could also be used.

3.2 Delay

The other most cited misconception is the huge delay in the encoding - decoding process. The delay incurred depends primarily on the information data rate and decoder speed. A simplistic approach is to consider that the end-to-end delay is 3BT where B is the information block size and T is the information bit period. This delay is composed from the transmitter delay, receiver delay and decoding delay, each assumed equal to BT. It was shown in [9] that there are techniques available to reduce the transmitter delay to a fraction of BT (eg. 1/4 or 1/8 of BT). For an FPGA implementation the decoder delay can also be reduced by parallel processing to less than T_D = 1 μs per coded symbol. This leaves us with a transmitter delay of say 0.25BT, a receiver delay of BT and a decoder delay of BT_D adding up to $B(1.25T + T_D)$. Most current standards target data rates above 1 Mbit/s which for a block B of 4000 bits translate in an end-to-end delay of less than 9 ms. For an ASIC implementation the T_D can be reduced to less than 0.3 μs per coded symbol which translates in an end-to-end delay of less than 6 ms.

3.3 Decoder Complexity

When it comes to complexity estimates, many authors start to sift through different formulations and simplifications of the MAP algorithm [10] and count additions and multiplications requirements [11] using complexity units per second. Caution is recommended when those numbers are considered due to the multitude of options to implement different algorithms.

In [12] a comparison in terms of performance, throughput, complexity and power consumption is made for the MAP, Log-MAP, Max-Log-MAP, Sliding MAP and SOVA algorithms. The conclusion is that a chip area of 2 mm^2 is sufficient to implement a turbo decoder for IMT-2000 for a throughput of 2 Mbit/s. The number of bits for the memory requirement as well as the number of decoding clocks for one frame (6144 information bit) decoding was investigated in [13]. Estimates range between 170 kbit and 950 kbit memory and between 15000 and 55000 clocks for different decoding algorithms.

A standard cell synthesis at 0.8 μm followed by automatic layout was used in [14] to estimate the VLSI complexity for the SOVA and MAP algorithms. For a serial implementation, 10 mm^2 and 13 mm^2 were required respectively.

A turbo decoder for a serial concatenated scheme with 2/3 and 3/4 codes that supports a 2 Mbit/s data rate was design in a 35 mm^2 area as described in [15]. The rate 2/3 decoder occupied 3 mm^2 and the rate 3/4 decoder occupied 5 mm^2. Most of the chip area was used by RAM (23.4 mm^2).

HSPICE simulations using 0.5 μm MIETEC technology was performed in [16] for a SISO module at a clock frequency of 1 GHz. The turbo decoder was shown it can run 10 iterations at 50 Mbit/s. The cost of the whole decoder was estimated at 575,000 transistors. It used 4 bit soft inputs, 5 bit branch metrics and 8 bit state metrics.

For DSP implementations, [17] reports on implementing a turbo decoder on the ADSP-21061 SHARC processor from Analog Devices, 40 MIPS version, that can achieve an average throughput greater than 70 kbit/s. No external memory is used in this implementation.

A different turbo decoder implementation on a Pentium II (400 MHz) PC can achieve a 773 kbit/s throughput as reported in [18].

The CAS 5093 chip implements five 8-state SOVA decoders in parallel and four 32x32 bit interleavers [19]. It can achieve 40 Mbit/s with a delay of 2318 bits. The "turbo4" chip [20] implements a single iteration of 2-state SOVA decoders in parallel with 64x32 bit interleaver.

STMicroelectronics has recently licensed turbo code technology from France Telecom and is producing a single 0.18 μm CMOS chip, STV0399, that incorporates both turbo coding and 8PSK modulation [21].

A turbo code of constraint length K_{tc} is estimated in [22] to require the same decoder complexity as a convolutional code with constraint length $K_{cc} = 3 + \log_2(Q) + K_{tc}$ where Q is the number of decoder iterations and Max-Log-MAP decoding is used. The convolutional code used by IS-95, $K_{cc} = 9$, can thus be fairly compared with a turbo code of $K_{tc} = 3$ and Q = 8 decoder iterations.

Analog decoders have a significantly less complexity than their digital relatives do. Very simple transistor circuits were used in ([23], [24]) to implement the basic engines of iterative decoders.

A decoder network was designed as analog network in [25] using 940 BJTs and 650 PMOS transistors in a standard 0.8μm BiCMOS technology. Its power consumption is 98 mW. With 90 ns decoding time per codeword, the analog decoder can achieve a data rate of 100 Mbit/s.

An analog tailbiting MAP decoder was implemented in analog VLSI using 0.25 μm BiCMOS technology [26]. It achieves a speed of 160 Mbit/s and the power consumption is 20 mW. It is estimated in [27] that the digital equivalent decoder would have a 3.3 times increase in overall performance degradation –assuming 8 bits resolution –, an 8 times higher power dissipation and 5.2 times larger area.

3.4 Error Floor

A few years ago there were many reports regarding the "error floor" of turbo codes. This was basically due to poor interleaver design and/or truncations in the decoding algorithm. Claims made today regarding the existing of error floor for turbo codes are due to ignorance or for political reasons. Both

Parallel and Serial concatenated schemes were shown that they could be designed without any error floor for whatever BER requirement [28]. In [29], a single PLD solution is used to implement a decoder for a double-binary circular recursive systematic convolutional component code used in a turbo scheme adopted for the DVB standard. No error floor appears regardless of the block size or coding rate down to PER of 10^{-8}. The same behaviour was reported in [7] for serial concatenated codes and target BER of 10^{-10}.

3.5 Memory Requirements

The amount of memory required by a 3GPP turbo decoder amounts to more than 80% of the chip area as reported in [30]. A nonlinear quantization of the extrinsic symbol is used to reduce its width from 6 to 3 bits, achieving a 13% reduction in overall turbo decoder complexity.

Techniques like sliding window ([31], [32]) can reduce significantly the amount of RAM required at the expense of a slight increased computational effort. The estimated RAM required for MAP decoding for a 16 state code with 6 bit state metrics is 96 bits per branch. For a 1000 bit block size, the estimated RAM is 96000 bit. The sliding window approach reduces this requirement to only 6000 bits which is no more than the storage requirements of a conventional Viterbi algorithm. In [32] it is concluded that a pair of 16 state concatenated decoders performing 4 iterations imposes double the processing load of a K = 7 Viterbi decoder and a pair of 4 state concatenated decoders performing 8 iterations imposes the same load as a K = 9 Viterbi decoder.

A MAP decoder that doesn't require external RAM and is based on a continuous sliding block algorithm is available from [33] as a BIT/MCS file for download into Xilinx Virtex field programmable gate arrays (FPGA). It targets iterative decoding of 3GPP or CCSDS turbo codes and can run at up to 99 Mbit/s decoding speed at variable coding rates.

4. Applications of Turbo Codes

4.1 Inmarsat

Inmarsat's multimedia service, ([4], [5], [6]) is a new service based on turbo codes and 16QAM that allows the user to communicate with existing Inmarsat-3 spot-beam satellites from a laptop-sized terminal at 64 kbit/s. The Narrowband Technology based on 16QAM and turbo-coding provides significant reduction (> 50%) in the required bandwidth for mobile satellite channels improving at the same time the satellite power efficiency.

The research into the performance of the coding and modulation scheme was described in [3]. A thorough investigation was performed in the non-linearities introduced by the high power amplifier (HPA) on the mobile terminal. Simulations and hardware measurements have shown that with minimum power amplifier back-off, optimal performance can be achieved with the 16QAM modulation. Of particular importance was the extra 0.5 dB coding gain that can be gained in higher order modulation schemes by mapping the information bits to the most protected positions in the QAM symbol. The turbo decoder was designed in VHDL using a single Altera FPGA. The whole turbo decoder fits on a daughter board shown in Figure 4.

The card can fit on any DSP board and can achieve a typical MAP decoder speed of 800 ns/bit, that is, an information data rate of 1.25 Mbit/s.

Further research in the coding and modulation technique showed that the data rates could be increased significantly by almost an order of magnitude.

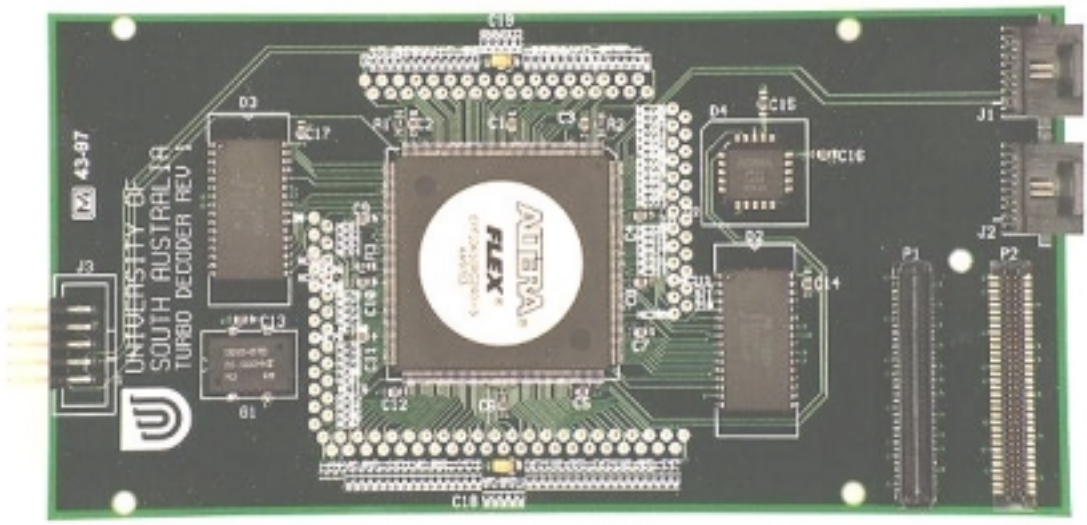

Figure 4: Turbo Decoder Card

4.2 DVB

The new European Digital Video Broadcasting (DVB) standard [34] has also adopted turbo codes for the return channel over satellite application (DVB-RCS). This standard allows a large number of small terminals to send "return" signals to a central gateway while they receive IP data (DVB/MPEG2) on the "forward" link. The users send small packets using multi-frequency time division multiple access (MF-TDMA) on demand assigned multiple access (DAMA). After the link is established, it is permanently available for the IP connection making efficient use of the satellite resources.

The turbo-coding scheme described in [35] allows transmission of data bit rates from 144 kbit/s up to 2 Mbit/s and uses a double-binary circular recursive systematic convolutional (CRSC) component codes. It can handle ATM (53 bytes) or MPEG (188 bytes) packets, the actual block sizes being variable from 12 to 216 bytes. The coding rates can be selected from 1/3, 2/5, 1/2, 2/3, 3/4, 4/5 and 6/7. A single chip solution, TC1000 turbo encoder/decoder, is already available on the market [29].

On going research is targeting the Digital Video Broadcasting – Satellite (DVB-S) [36] and Digital Satellite News Gathering (DVB-DSNG) [37]. The high target data rate around 45 Mbit/s requires higher order modulation schemes. Preliminary studies [38] have shown that turbo codes can achieve a 10-20% increase in bit rate and at the same time 1.5 to 2 dB increase in C/N gain. However, migration to these schemes, which are not backward compatible, has commercial and operational implications.

4.3 Deep-Space Communications

Maybe the most suitable application of turbo codes is in deep-space communications ([39], [40]). This is firstly because using very large interleavers can maximize the turbo coding gain, the delay not being an issue at all. Secondly, more than two elementary encoders can be combined in many efficient ways to create a very powerful low rate turbo code at a slight increase in complexity. The operating SNR of such coded schemes can be a negative number well below the current synchronization capabilities of the receiver.

The European Space Agency (ESA) has investigated the potential use of turbo codes in a series of deep-space missions like Rosetta, Mars Express and SMART-1 [41].

4.4 CCSDS

The new standard of the Consultative Committee for Space Data Systems (CCSDS) establishes a common Recommendation for space telemetry channel coding systems [42]. The telemetry channel coding concept described in the Recommendation represents the baseline for spacecraft-to-ground data communication. It allows the development of compatible derived standards for the flight and ground systems [43].

The recommended codes include turbo codes based on 16 state recursive convolutional codes with selectable coding rates from 1/2, 1/3, 1/4, and 1/6. It can use large interleaver blocks, from 1784 bits to 16384 bits. The new standard outperforms with 1.5 to 2.8 dB the old CCSDS standard based on concatenated convolutional code and Reed-Solomon code [40].

4.5 DSN

NASA's next-generation of deep-space transponder will support turbo codes. The implementation of turbo decoders in the Deep Space Network (DSN) is planned by 2003 [44]. This development is part of a strategic planning through the year 2010 which targets improvements in RF, Ka-Band and optical communications systems.

4.6 UMTS

The advantage of turbo codes over conventional codes was thoroughly demonstrated one year after the invention of turbo codes in joint detection code division multiple access (JD-CDMA) mobile radio and GSM/DCS 1800 systems ([45], [46]).

Recently, the technical specification for the Universal Mobile Telecommunications System (UMTS) has been a Third Generation Partnership Project (3GPP) proposal that included turbo codes in the multiplexing and channel coding specification ([47], [48], [49]). The IMT-2000 represents the third-generation mobile radio systems worldwide standard. It targets a very high bit rate suitable for wireless multimedia communications. It provides for circuit-switched and packet-switched services such as IP traffic and real-time video with good voice quality and improved spectrum efficiency. The concept of Virtual Home Environment will enable the user’s handset to keep application’s aspect while roaming all over the world.

Many of the turbo decoders described in Section 3.3 target this particular application.

4.7 DAB

A new satellite Direct Audio Broadcasting (DAB) scheme using turbo codes was investigated in [54] and achieved 3.2 dB and 4.5 dB improvements over the current standard in AWGN and Rayleigh fading channels respectively.

DAB was introduced in U.S.A. in 1996 and provides full continental coverage of CD-quality digital radio programs. The S-band mobile channel is characterized by signal shadowing and multi-path from man-made and natural structures. The turbo code investigated is the same proposed in the CCSDS standard with an interleaver size of 8920. The scheme used a code combiner technique which, if both code rate ½ transmitted signals are available at the receiver, the output of the combiner becomes a powerful code rate ¼ signal.

4.8 Magnetic Recording Channels

Standard protocols for disk drivers using turbo codes have been investigated in [50], [51], [52] and [53]. The superiority of turbo codes over trellis and spectral null codes in partial response class 4 (PR4) channels was proven for very high coding rates up to 16/17. Coding gains of 7.1 dB relative to the uncoded case are achieved at a BER = 10^{-5} for rate 4/5 and 8/9 codes and 6.5 dB for rate 16/17 codes.

4.9 INTELSAT

INTELSAT is currently investigating the application of turbo codes to their digital services for rates up to 2 Mbit/s [7]. INTELSAT offers the IDR/IBS services based on convolutional codes in conjunction with Reed-Solomon (RS) outer coding. A new serial concatenated scheme was developed and implemented in FPGAs in a *Turbo Codec - QPSK Modem* proof-of-concept hardware. It can achieve a BER of 10^{-10} at E_b/N_0 = 2.0 dB for coding rate ½ and at E_b/N_0 = 3.3 dB for coding rate ¾. The *Turbo Codec - QPSK Modem* can be configured for minimum end-to-end delay applications or for maximum coding gain by using interleaver sizes up to 64 kbits. The number of iterations can also be programmed from 1 to 16. No RS outer coding is required and no flattening of the BER curve is noticeable down to the target BER of 10^{-10}.

A photo of the *Turbo Codec - QPSK Modem* in Figure 5 and a BER curve for rate ½ in Figure 6.

Figure 5: *Turbo Codec – QPSK Modem*

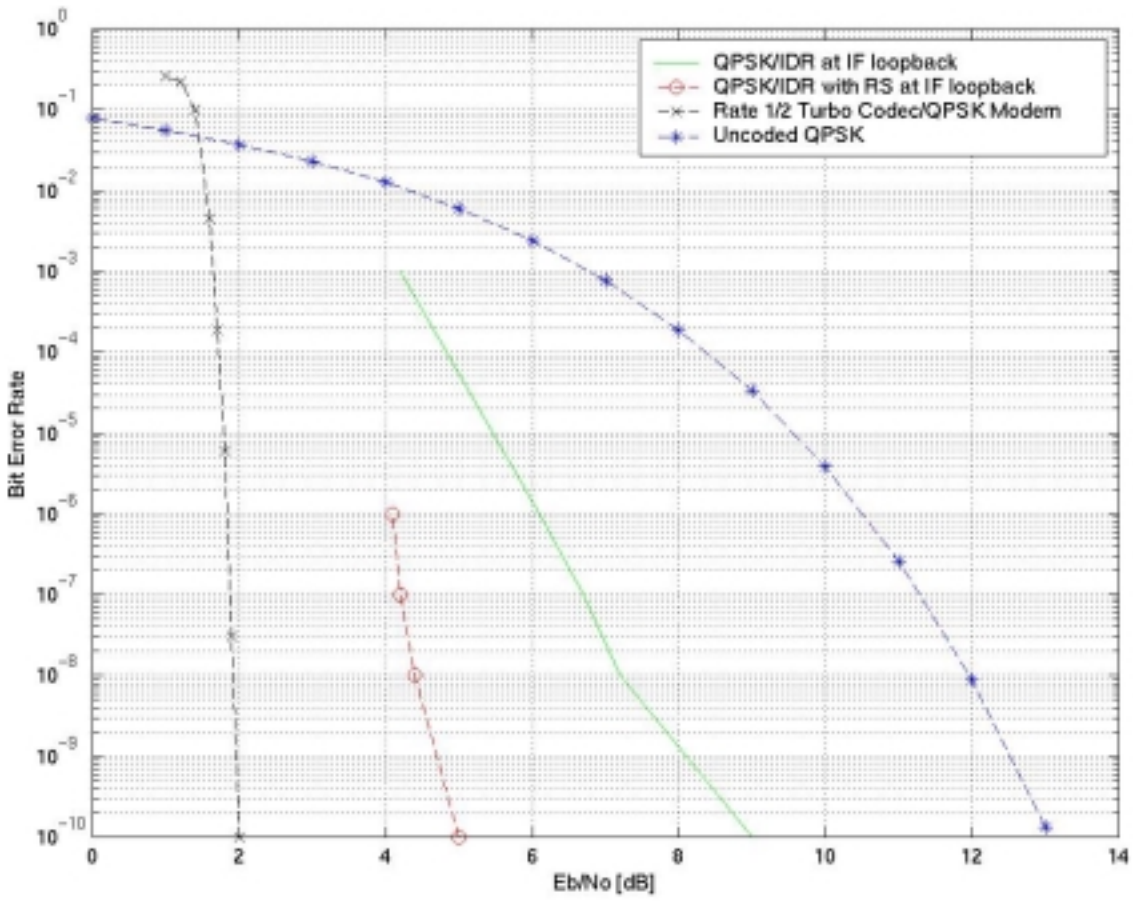

Figure 6: BER performance of Rate ½ *Turbo Codec – QPSK Modem*

5. ADSL

5.1 Turbo Coding Solution

Asymmetric Digital Subscriber Lines (ADSL) using Discrete Multitone (DMT) is another potential application of turbo codes. The standard described in [55] employs an outer Reed-Solomon (RS) code and an inner constellation encoder, which may or may not include a trellis code. Recent studies ([56], [57], [58]) have shown that the inner encoder can be replaced with a turbo encoder to achieve significant coding gains. Given that the standard specifies an RS encoder/decoder must be employed for the uncoded bits in each DMT symbol, the proposed turbo code target is a BER of 10^{-7}.

A solution based on a parallel concatenated turbo coding scheme was proposed in ([59], [60]). This proposal has the following advantages:

1. When turbo codes are used in conjunction with very high order modulations, the complexity of estimating the bit probability from the received symbol becomes a significant problem. The independent mapping has the advantage of reduced number of computations/memory required for each bit estimate from the received symbol at no

significant penalty in performance. For example, for a 1024QAM constellation made of two independent unidimensional 32PAM signals, only 32 possible transmitted symbols are compared to estimate the bit probability for each bit in the 32PAM symbol. If no independent I and Q mapping is used, then all 1024 possible transmitted symbols have to be used to estimate each bit probability. The process has to be repeated for every received symbol.

2. The bit mapping within a QAM symbol can place either the information bits or the parity bits in the most protected positions of the QAM symbol for coding rates. As confirmed in ([3], [61]), for low coding rates and 16QAM/64QAM modulation, the mapping of the information bits in the most protected position gains 0.5 dB in an AWGN channel at BERs higher than 10^{-8} when compared with mapping the parity bits into the most protected position. This is due to the higher sensitivity of turbo codes to errors that appear in the information bits rather than in the parity bits. However, when different channels are considered, like impulse noise channel, more simulation results have indicated that more protection is required for the parity bits.

3. The parallel concatenation is known to perform closer to capacity than the serial concatenation, at similar complexity/delay and for relatively low BER with the crossover point around 10^{-6} or 10^{-7} [62]. The extra coding gain of the proposed parallel scheme gives around 0.3 to 0.5 dB improvement over serial concatenation schemes at the BER of interest.

4. The proposed scheme achieves a target BER of 10^{-7} at as close as 0.8 dB from capacity as described in Section 5.2.

5. The proposed scheme is based on convolutional codes rather than block codes. This means that the block size is not constrained to a particular size as in the case of block codes (which include turbo block codes, turbo product codes, low density parity-check codes, etc). This variable block size can be easily matched by a variable interleaver suitable for the particular channel conditions.

6. It is well known that the impulse noise degrades significantly the performance of any coded scheme. It was shown in [63] that if the impulse noise samples can be located exactly and erased (set to zero in the turbo decoder) the performance of a turbo coded scheme can be further improved. This is possible by monitoring several pilot tones to provide a reliable estimation of the impulse noise.

7. A further improvement could be achieved if Automatic Repeat Request (ARQ) is used in the system ([64], [65]). This will eliminate completely the rare events when the turbo decoder fails to correct a block due to extremely high impulse noise.

5.2 Example for independent I & Q mapping.

In order to understand the advantages of the scheme proposed in [59], this section presents an example for the 16QAM constellation. For a 16QAM scheme, the symbol $u^k = (u_1^k, u_2^k, u_3^k, u_4^k)$, is sent through the channel at time k and the point r^k in a two dimensional space is received.

The 16QAM symbol is defined by the I and the Q components which are 4AM signals. Each signal is modulated independently by two bits. It is assumed that at time *k*, u_1^k and u_2^k modulate the I component and u_3^k and u_4^k modulate the Q component of a 16QAM scheme.

At the receiver, the I and Q signals are treated independently in order to take advantage of the simpler formulae for the 4 bit-LLR values. The mapping of the information bit is made to the most protected bit in each dimension (u_1^k for the I signal and u_3^k for the Q signal) as it is shown in Figure 7 and Figure 8.

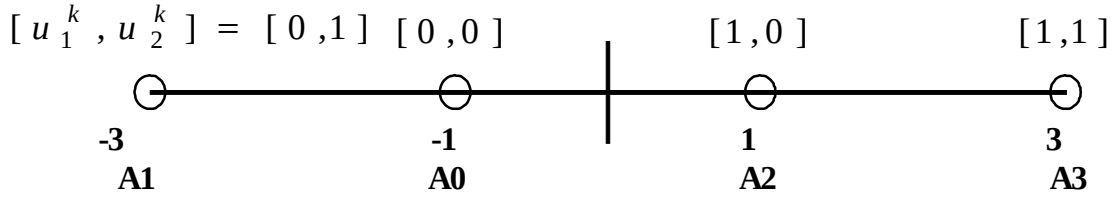

Figure 7: Mapping in the I dimension

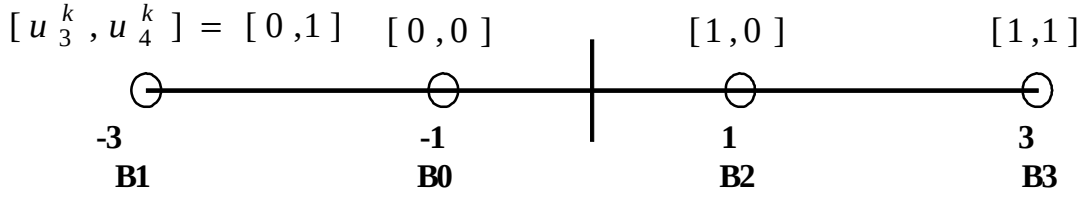

Figure 8: Mapping in the Q dimension

The puncturing and bit mapping is shown in Table 1 for the first 8 data bits. The first bit in each pair for the I and Q is the most significant bit. This simple model was used as a first step to understand this process. It assumes a transmitter delay of one block due to the interleaving process.

Table 1: Puncturing and Mapping for Rate ½ 16QAM

Information bit (d_I)	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8
parity bit (p_I)	p_1	-	p_3	-	p_5	-	p_7	-
parity bit (q_I)	-	q_a	-	q_b	-	q_c	-	q_d
4AM symbol (I)	(d_1, p_1)		(d_3, p_3)		(d_5, p_5)		(d_7, p_7)	
4AM symbol (Q)	(d_2, q_a)		(d_4, q_b)		(d_6, q_c)		(d_8, q_d)	
16QAM symbol	(d_1, p_1, d_2, q_a)		(d_3, p_3, d_4, q_b)		(d_5, p_5, d_6, q_c)		(d_7, p_7, d_8, q_d)	

For an AWGN channel, the following LLRs need to be evaluated from the received I signal:

$$LLR(u_1^k) = \log \frac{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(I^k - a_{1,i}^k)^2]}{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(I^k - a_{0,i}^k)^2]} =$$

$$= \log \frac{\exp[-\frac{1}{2\sigma^2}(I^k - A_2)^2] + \exp[-\frac{1}{2\sigma^2}(I^k - A_3)^2]}{\exp[-\frac{1}{2\sigma^2}(I^k - A_0)^2] + \exp[-\frac{1}{2\sigma^2}(I^k - A_1)^2]} \qquad \text{(eq. 5-1)}$$

$$LLR(u_2^k) = \log \frac{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(I^k - a_{1,i}^k)^2]}{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(I^k - a_{0,i}^k)^2]} =$$

$$= \log \frac{\exp[-\frac{1}{2\sigma^2}(I^k - A_1)^2] + \exp[-\frac{1}{2\sigma^2}(I^k - A_3)^2]}{\exp[-\frac{1}{2\sigma^2}(I^k - A_0)^2] + \exp[-\frac{1}{2\sigma^2}(I^k - A_2)^2]} \qquad \text{(eq. 5-2)}$$

For an AWGN channel, the following LLRs need to be evaluated from the received Q signal:

$$LLR(u_3^k) = \log \frac{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(Q^k - a_{1,i}^k)^2]}{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(Q^k - a_{0,i}^k)^2]} =$$

$$= \log \frac{\exp[-\frac{1}{2\sigma^2}(Q^k - B_2)^2] + \exp[-\frac{1}{2\sigma^2}(Q^k - B_3)^2]}{\exp[-\frac{1}{2\sigma^2}(Q^k - B_0)^2] + \exp[-\frac{1}{2\sigma^2}(Q^k - B_1)^2]} \qquad \text{(eq. 5-3)}$$

$$LLR(u_4^k) = \log \frac{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(Q^k - a_{1,i}^k)^2]}{\sum_{i=1}^{2} \exp[-\frac{1}{2\sigma^2}(Q^k - a_{0,i}^k)^2]} =$$

$$= \log \frac{\exp[-\frac{1}{2\sigma^2}(Q^k - B_1)^2] + \exp[-\frac{1}{2\sigma^2}(Q^k - B_3)^2]}{\exp[-\frac{1}{2\sigma^2}(Q^k - B_0)^2] + \exp[-\frac{1}{2\sigma^2}(Q^k - B_2)^2]} \qquad \text{(eq. 5-4)}$$

The above LLRs are used as inputs to the turbo decoder.

It can be easily noticed that the above summations are over 2 symbols due to the independent mapping in each dimension. If a two dimensional mapping is used, the above summations need to be over 8 symbols, that is, half the number of constellation symbols. In this case, these numbers grow significantly for very high order constellations. Therefore, there is a substantial reduction in the computational effort by using the independent mapping in each dimension.

5.3 Example for reduced transmitter delay

This Section describes a particular mapping of the coded bits into the QAM symbols that can significantly reduce the transmitter delay as mentioned in Section 3.2. Two cases are described, one for Rate 4/6 64QAM and another for Rate 12/14 16384QAM.

5.3.1 Rate 4/6 64QAM

For a 4/6 coding rate, let's assume that a block N of 24 information bits is used. The information bits are encoded at the same time they are available to produce 6 parity ***p*** bits (N/4) after puncturing. These bits are produced at the same time as the information bits are received. After all information bits are received, the interleaved data is re-encoded again to produce 6 parity ***q*** bits (N/4). We assume that the mapping used is as shown in Table 2. The 36 coded bits (3N/2) are mapped six at a time in six 64QAM symbols (N/4).

Table 2: Puncturing and Mapping for Rate 4/6 64QAM

information bit (d)	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8
parity bit (p)	p_1	-	-	-	p_5	-	-	-
parity bit (q)	-	-	q_a		-	-	q_b	-
8AM symbol (I)	(p_1, d_1, d_2)				(p_5, d_5, d_6)			
8AM symbol (Q)	(q_a, d_3, d_4)				(q_b, d_7, d_8)			
64QAM symbol	(p_1, d_1, d_2, q_a, d_3, d_4)				(p_5, d_5, d_6, q_b, d_7, d_8)			

If the parity bits, ***p*** and ***q***, are mapped on the most protected positions in each dimension, the six parity ***q*** bits (N/4) can be mapped two in a symbol in the last three (N/8) 64QAM symbols. This means that once half (4N/8) of the 24 information bits are received, the transmitter process can start, reducing the transmitter delay to 50%. This process is illustrated in Table 3. This transmitter delay could be reduced even further at the cost of a small reduction in performance. If the parity bits ***q*** are mapped together, six per symbol, they can be transmitted in N/24 symbols, that is in the last QAM symbol. This in effect translates into a transmitter delay of only N/6 bits or approximately 17%.

Table 3: Transmitter Delay for Rate 4/6 64QAM

Time index	Information bit	Parity *p*	Parity *q*	64QAM symbol
1	d1	p1	-	-
2	d2	-	-	-
3	d3	-	-	-
4	d4	-	-	-
5	d5	p5	-	-
6	d6	-	-	-
7	d7	-	-	-
8	d8	-	-	-
9	d9	p9	-	-
10	d10	-	-	-
11	d11	-	-	-
12	d12	-	-	-
13	d13	p13	-	$(p_1, d_1, d_2, p_5, d_3, d_4)$
14	d14	-	-	
15	d15	-	-	
16	d16	-	-	
17	d17	p17	-	$(p_9, d_5, d_6, p_{13}, d_7, d_8)$
18	d18	-	-	
19	d19	-	-	
20	d20	-	-	
21	d21	p21	-	$(p_{17}, d_9, d_{10}, p_{21}, d_{11}, d_{12})$
22	d22	-	-	
23	d23	-	-	
24	d24	-	-	
25	All six ***q*** bits can now be computed at a very fast speed			$(q_a, d_{13}, d_{14}, q_b, d_{15}, d_{16})$
26	-	-		
27	-	-		
28	-	-		
29	-	-		$(q_c, d_{17}, d_{18}, q_d, d_{19}, d_{20})$
30	-	-		
31	-	-		
32	-	-		
33	-	-		$(q_e, d_{21}, d_{22}, q_f, d_{23}, d_{24})$
34	-	-		
35	-	-		
36		-		

5.3.2 Rate 12/14 16384QAM

For a 12/14 coding rate, let's assume that a block of N information bits is used. The information bits are encoded at the same time they are available to produce N/12 parity ***p*** bits after puncturing. These bits are produced at the same time as the information bits are received. After all information bits are received, the interleaved data is re-encoded again to produce N/12 parity ***q*** bits. The N+N/12+N/12 = 7N/6 coded bits are mapped 14 at a time in a 16384QAM symbol.

If the parity bits, ***p*** and ***q***, are mapped on the most protected positions in each dimension, the N/12 parity ***q*** bits can be mapped two in a symbol in the last (N/24) 16384QAM symbols. This means that the transmitter process can start exactly after 6N/24 = N/2 bits are received from the source reducing the transmitter delay again to 50%.

As in the previous example, the transmitter delay could be reduced even further at the cost of a small reduction in performance. If the parity bits $\boldsymbol{q}$ are mapped together, 14 per symbol, they can be transmitted in the last N/(12*14) symbols. This in effect translates to a transmitter delay of only 12N/168 = N/14 bits or approximately 7%.

Figure 9 shows some simulation results for the Rate 4/6 64QAM case with a block of 10400 bits using an S-type interleaver. The case using the mapping of the information bits in the most protected position achieves better performance than the case using the mapping the parity bit is placed in the most protected position for BER higher than 10^{-8}.

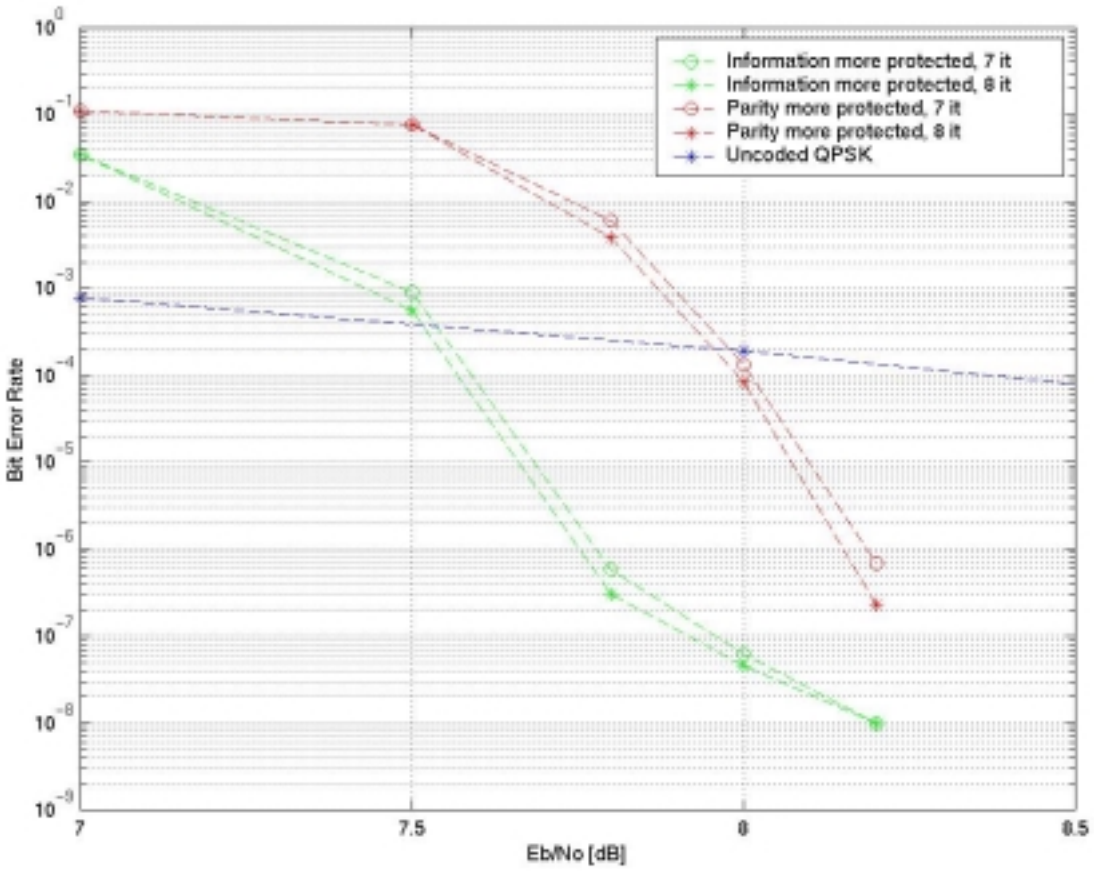

Figure 9: Simulation results

Simulation results are shown in Table 4 for different constellation sizes. The required E_b/N_0 represents the minimum E_b/N_0 to achieve a BER of 10^{-7}. It is clear that, function of the interleaver size, the performance of turbo codes is between 0.8 and 2.5 dB from capacity.

Table 4: Performance Results

Spectral efficiency	Coding Rate	Modulation	Interleaver size	Required E_b/N_0 [dB]	QAM bound [dB]
2	1/2	16QAM	2,048	4.2	2.1
2	1/2	16QAM	32,768	2.9	2.1
3	3/4	16QAM	4,098	5.8	4.6
4	4/6	64QAM	4,096	8.3	6.6
5	5/8	256QAM	5,120	11.8	9.0
6	6/8	256QAM	6,144	14.2	11.7

6. Conclusion

This paper presented the advantages of using turbo codes in modern communication systems. This information is provided to the committee to show that turbo codes can considerably improve the performance and hence they are very successful in the standard community. It is proposed that, for G.992.1.bis, G.992.2.bis and G.vdsl recommendations, the use of Turbo Codes in the transmitter to be mandatory and allow the receiver to select this option in G.hs. The reason to include this in the standard is to allow manufacturer interoperability and provide improvements over Trellis Codification Modulation.

7. Summary

We recommend that G.992.1.bis and G.992.2.bis use Turbo Codes to reach longer loops or increase the throughput of the system.

1. Agenda Item: G.992.1.bis issue 4.2, G.992.2.bis issue 1.4 and G.vdsl issue 11.17.
2. Expectations: The committee accepts the baseline text described in this paper.

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