# VOCAL

Space Application Development Board

The Space Application Development Board (SADB-C6727B) enables developers to implement systems using standard and custom algorithms on processor hardware similar to what would be deployed for space in a fully radiation hardened (rad-hard) design. The SADB-C6727B is devised to be similar to a space qualified rad-hardened system design using the TI SMV320C6727B-SP DSP and high-rel memories (SRAM, SDRAM, NOR FLASH) from Cobham. The VOCAL SADB-C6727B development board does not use these high reliability space qualified components but rather implements various common bus widths and memory types/speeds for algorithm development and performance evaluation.
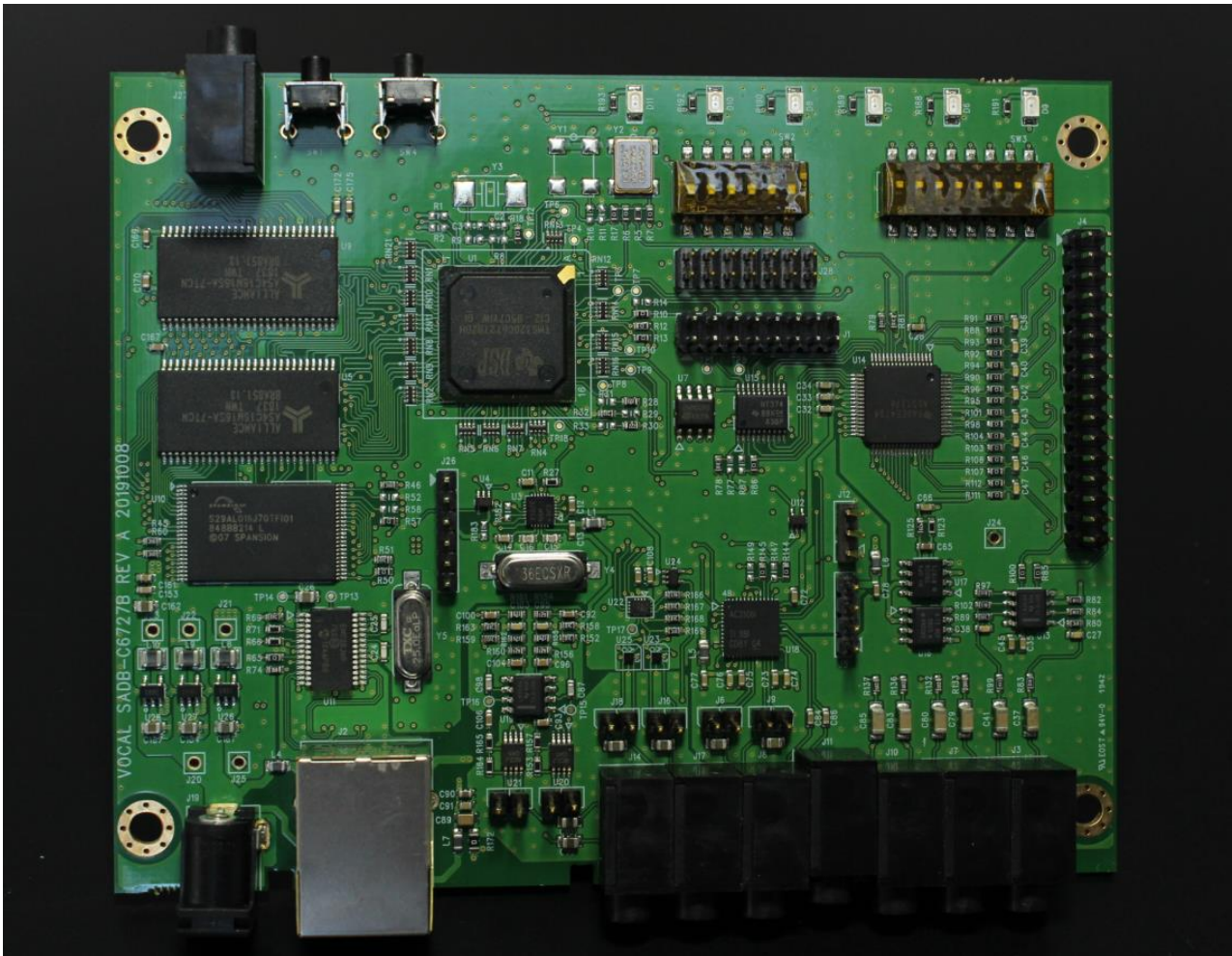
Audio inputs are handled by a TI ADS1278 high speed multichannel analog-to-digital converter (ADC) which has a variant qualified for space operation. Audio outputs may be generated from digital signal Pulse Density Modulation (PDM) or Pulse Width Modulation (PWM) signals to avoid the need for a space qualified digital-to-analog converter (DAC) hardware or a traditional audio codec circuit. A commercial grade AIC3106 audio codec is provided for algorithm development and for comparison of audio performance to PDM/PWM generated audio signals. Digital microphones (PDM or I2S formats) can be sampled by the processor directly or by the AIC3106 audio codec (PDM format only). Digital audio inputs/outputs can also be connected to other processors (using the McASP signals directly).

Both SRAM and SDRAM memories are supported via configuration resistors to allow for developing and benchmarking algorithms using either 16-bit wide or 32-bit wide busses (also via configuration resistors). Similarly the parallel NOR flash can operate with either 8-bit or 16- bits busses. Large SDRAM can be easily accessed while the high address bits of SRAM and FLASH are page addressed via processor GPIO signals. Both the parallel NOR flash and an I2C EEPROM may be used a processor boot devices.

The Ethernet MAC/PHY connects via SPI and is used to simulate off-processor communications. This is not likely to be directly used in space environments but can be used to approximate an Ethernet/IP based communications network. A serial UART connected via I2C is used for diagnostic/development purposes. JTAG is also supported but generally is insufficient for monitoring a real-time running system which is why UART serial data is supported.
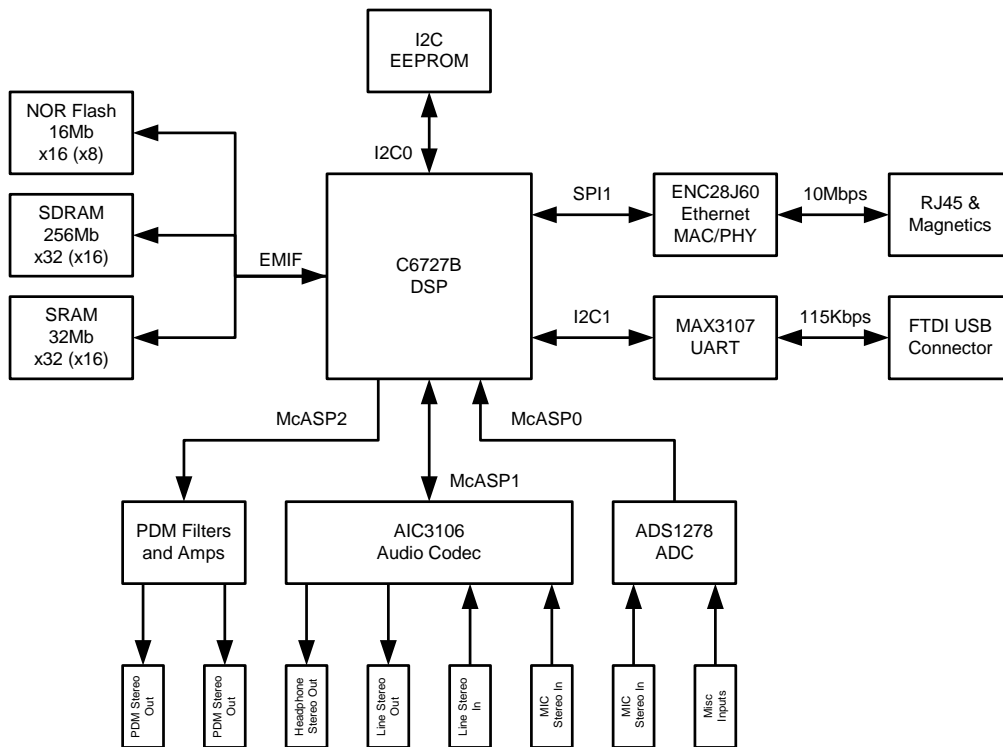
(Not included in SADB datasheet. Belongs to a different product.)

Product configurations (please see diagrams on next page):

      3 Analog Ports with GPIO controls and one FXO Phone Port
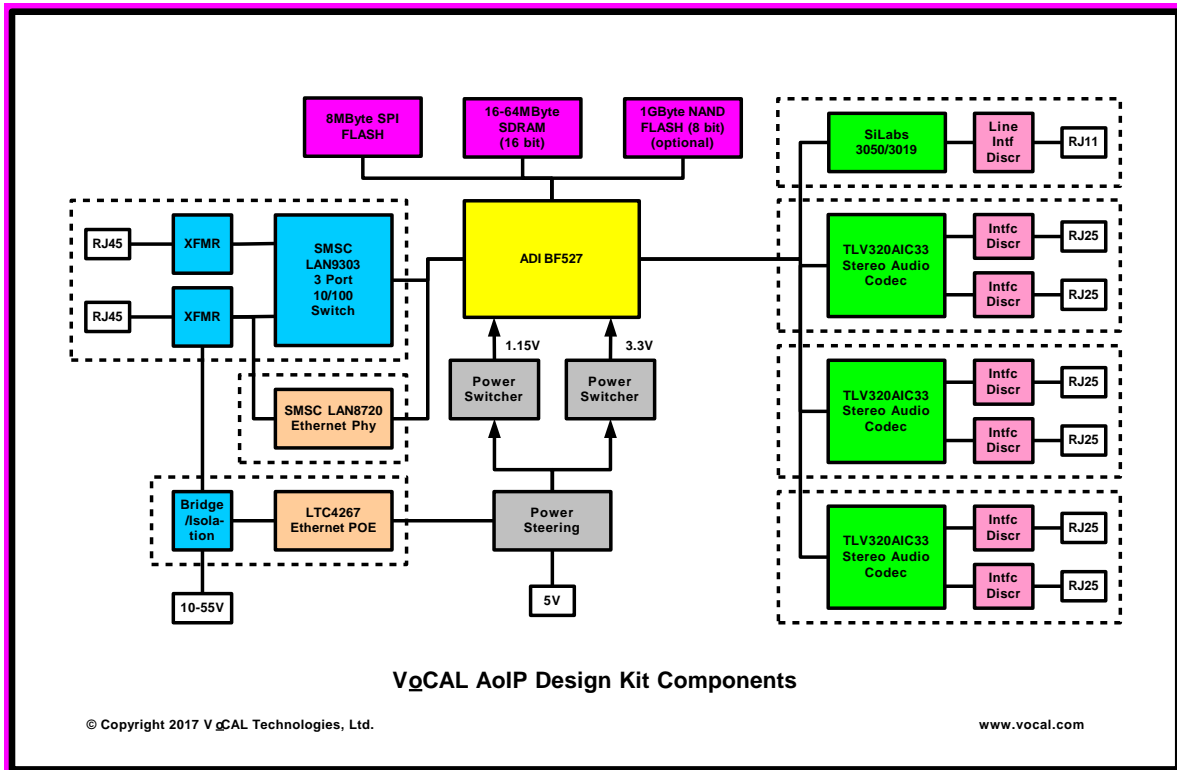   4 Analog Ports with GPIO controls
      6 Analog Ports with one FXO Phone Port
      8 Analog Ports
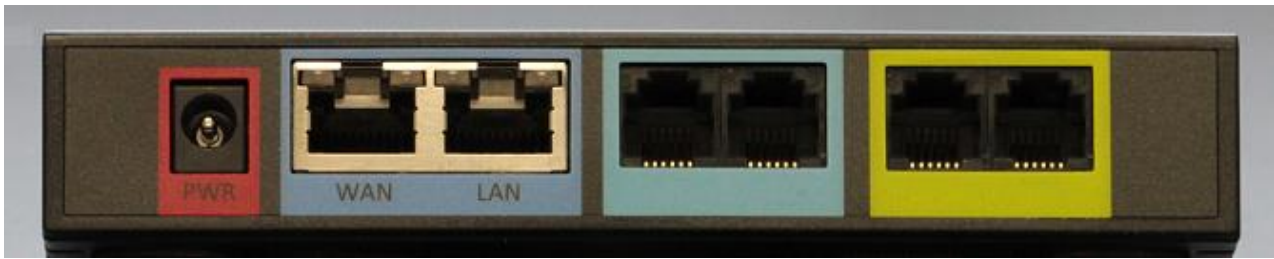   1 or 2 Ethernet with optional POE
      5 volt wall adapter standard
      10-55 volt isolated power option

VoCAL AoIP Design Kit Components

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The designs include options for GPIO control signals and RSSI signal monitoring. GPIO signals are protected and configurable for driving PTT (push to talk) and receiving COS/COR (carrier on squelch/receive) signals. Alternate control signals may be configured for I2C operation and/or an I2C Async serial UART using additional circuitry*. Control signals may be optically or relay isolated*. Analog signals are single-ended and may be converted to isolated 600 ohms*. Digital MEMS microphones may be supported as an alternate use of GPIO signals with synchronous sampling of all channels.

* - Requires external circuitry or a daughter board add-on to reference board.

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Connectors (left to right):

      5.5/2.1mm barrel connector for 5VDC or optional 10-50V isolated power[+]
      RJ45 Ethernet with optional POE
      RJ45 Ethernet (optional)
      RJ25 Analog Port 3 (channels 6 and 7 for L and R respectively)
      RJ25 Analog Port 2
      RJ25 Analog Port 1
      RJ11 Telephone FXO Port

+ - Optional isolated power supply also supports locking barrel connector. Requires resistor straps and eliminates Ethernet POE.

For all Analog Ports (RJ25 - 6 position, 6 contact):

      Pin 1 – GPIO IN, I2C SDA, I2C SCL, +3.3V or +5V
      Pin 2 – Audio out L
      Pin 3 – Audio in L
      Pin 4 – Audio in R, GPIO IN, I2C SDA, RSSI
      Pin 5 – GPIO OUT, Audio out R, I2C SCL, Processor GPIO/IRQ
      Pin 6 – Ground

In case of multiple signals, the factory default signal is shown first. Alternative signals usually require reconfiguration of strapping resistors.

GPIO IN may be used as a secondary output. As an input, GPIO IN is buffered with Schmitt logic by default, and may drive the base of an NPN collector (for voltage isolation) or maybe a direct input. GPIO outputs are buffered by a high voltage (40V) open NPN collector by default or maybe a direct output.

Audio inputs may be biased for powering Electret or MEMS analog microphones using resistor straps and software configuration (none, 2, 2.5 or 3.1V bias). Audio inputs/outputs $2V_{p-p}$ or $0.707V_{rms}$ max (0dB). Audio input voltage divider are configurable with resistors.

I2C signals (SCL and SDA) may be used directly externally or connected to additional I2C compatible devices such as an I2C UART for external asynchronous connections.

Processor GPIO/IRQ is intended for use only by internal expansion daughter cards.

For Telephone FXO Port (RJ11 – 6 position, 2 contact):

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Pin 1 –
Pin 2 –
Pin 3 – Tip
Pin 4 – Ring
Pin 5 –
Pin 6 –

Example Radio Configuration – One UHF/VHF AM/FM radios using RSSI or COR for receiver activation:

Pin 1 – GPIO COR input
Pin 2 – Audio out
Pin 3 – Audio in
Pin 4 – RSSI input
Pin 5 – GPIO PTT output
Pin 6 – Ground

Example Dual Radio Monitor Configuration – One port to two FM radios using VOX/VAD for receive activation:

Pin 1 – GPIO PTT R
Pin 2 – Audio out L (connects to both audio transmit signals)
Pin 3 – Audio in L
Pin 4 – Audio in R
Pin 5 – GPIO PTT L
Pin 6 – Ground

Example Beamformer Configuration – dual microphones (analog or digital) on each port:

Pin 1 – Digital stereo microphone data (sampled on alternate clock edges)
Pin 2 – Audio out (optional)
Pin 3 – Analog microphone in L
Pin 4 – Analog microphone in R
Pin 5 – Digital microphone clock
Pin 6 – Ground

ED-137B E&M Daughter Board Expansion - Attaches internally to the AoIP reference board and supports four ports of the following:

Pin 1 – SB (M Lead return) [#]
Pin 2 – M Lead (COR) with configurable polarity and ground/return[#]
Pin 3 – RX Audio+ (protected and 600ohm isolated)
Pin 4 – TX Audio+ (protected and 600ohm isolated)
Pin 5 – TX Audio-
Pin 6 – RX Audio-
Pin 7 – E Lead (PTT) with configurable polarity and ground/return[#]
Pin 8 – SG (E Lead return) [#]

- Supports E&M Types I to V by configuration jumper or soldered 0 ohm resistors

Reference Design Kit

The VOCAL SADB Reference Design Kits support the following licensable capabilities:

Technical Specifications

Voice-over-IP (VoIP) protocols
  SIPv2 - Session Initiation Protocol (RFC 3261, 3262, 3263, 3264)
  SDP - Session Description Protocol (RFC 4566)
  RTP - Real-Time Protocol (RFC 3550, 3551)
  RTCP - Real-Time Control Protocol (RFC 3550)
  RFC 4733 X-NSE Tone Events for SIP/RTP
  RFC 4733 AVT Tone Events for SIP/RTP
  STUN - Simple Traversal of UDP over NATs (RFC 3789)

Optional VoIP Security Protocols
  SIPS - SIP Secure using TLS (RFC 3261)
  SRTP - Secure Real-time Transport Protocol (RFC 3711, 4568)
  MKI - Master Key Identifier (part of RFC 3711)
  AES - Advanced Encryption Standard - supports 128/195/256 bit keys
  HMAC – Authentication

Network Protocols
  IPv4 - Internet Protocol Version 4 (RFC 791)
  TCP - Transmission Control Protocol (RFC 793)
  UDP - User Datagram Protocol (RFC 768)
  ICMP - Internet Control Message Protocol (RFC 792)
  RARP - Reverse Address Resolution Protocol (RFC 903)
  ARP - Address Resolution Protocol (RFC 826)
  DNS- Domain Name Server
  DHCP Client - Dynamic Host Control Protocol (RFC 2131)
  NTP - Network Time Protocol (RFC 1305)
  SNTP - Simple Network Time Protocol (RFC 2030)
  HTTP - HyperText Transfer Protocol
  TFTP - Trivial File Transfer Protocol (RFC 1350)
  PPPoE - Point to Point Protocol over Ethernet (RFC 2516)

Voice Codecs
  G.711 - Pulse Code Modulation
  G.722 - Wideband ADPCM
  G.722.1 - 24k and 32k bps 7kHz Wideband
  G.722.2 - GSM-AMR-WB
  G.723.1 - 6.4 and 5.3 kbps ACELP/MP-MLQ
  G.726 - 16, 24, 32 and 40 kbps ADPCM
  G.728 - 16 kbps LD-CELP
  G.729 - 8 kbps CS-ACELP
  G.729A - 8 kbps CS-ACELP Low Complexity
  G.729B - Silence Detection/Comfort Noise Generation
  G.729D - 6.4 kbps CS-ACELP
  G.729E - 11.8 kbps CS-ACELP
  GSM-FR - GSM 06.10 Full Rate Vocoder
  GSM-AMR NB - GSM 06.90 Adaptive Multi-Rate
  GSM-AMR WB - Wideband Adaptive Multi-Rate
  iLBC - Internet Low Bitrate Codec
  OPUS - 16KHz SILK, 22/24KHz CELT
  Speex – 8 kbps CELP
  MELPe - 2400/1200/600 bps Codec
  TSVCIS - Tactical Secure Voice (Wideband MELPe)
  LPC10 and CVSD - Legacy Voice Codecs

Telephony
  Q.24 DTMF Generation with Zero Crossing Cutoff
  Q.24 DTMF Detection exceeding Bellcore Specifications
  Configurable Tone Generation for 4 Sets of Frequencies and 4 Sets of On/Off Cadence
  Programmable Precise Tone Detectors

Line Echo Cancellation
  G.168 Line Echo Cancellation
  16/32/64 ms Echo Length
  Nonlinear Echo Suppression (ERL greater than 28 dB for f = 300 to 3400 Hz)
  Double-Talk Detection

Acoustic Echo Cancellation
  Full Duplex Speakerphone
  Narrow and Wideband Operation (8Khz and 16KHz)
  Adjustable Tail Length (128 ms typical, 256 ms max)
  Nonlinear Echo Processing with Comfort Noise Generation
  Full Duplex Operation with Noise Reduction
  Double-Talk detection, Low Divergence during Double Talk

Noise Processing
  Dual/Multi-Microphone Adaptive Noise Cancellation
  Single Channel Noise Reduction
  Active Noise Cancellation to identify and remove repetitive noise signals
  Frequency Domain Noise Reduction
  18dB Noise Reduction (typical)
  Approximate 20msec Delay

Audio Beamforming
  Audio Beamforming (four or more mics)
  Audio Null Forming
  Direction of Arrival Estimation
  Audio Beam Steering

Voice Quality Enhancements
  Automatic Gain Control
  Voice Compressor
  Multiband Equalizer
  Automatic Delay Estimation
  Battle Field VOX
  Voice Activity Detection
  Noise Gating
  Wind Noise Reduction
  Click Noise Removal
  VAD/DTX/CNG as per SCIP 210 Appendix B